Software Hardware Approaches for Reducing the Energy Consumption of Embedded Systems

Faculty Name

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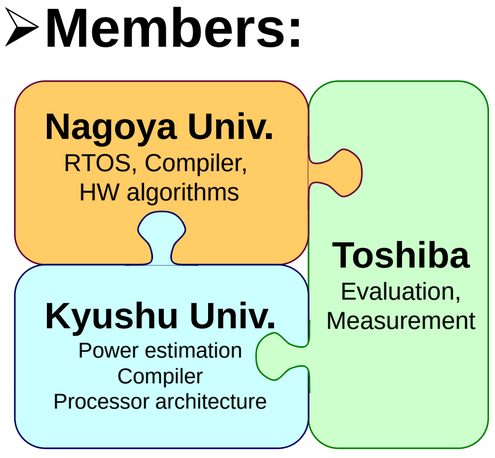
Project Overview

- **Sponsor:** Japan Science and Technology Agency (JST)
- **Goal:** Improving performance per energy by 2 orders of magnitude
- **Target:** Processor-based embedded systems
- **Our approach:** Cooperating HW & SW optimization considering tradeoffs among energy, performance and QoS
- **Members:**

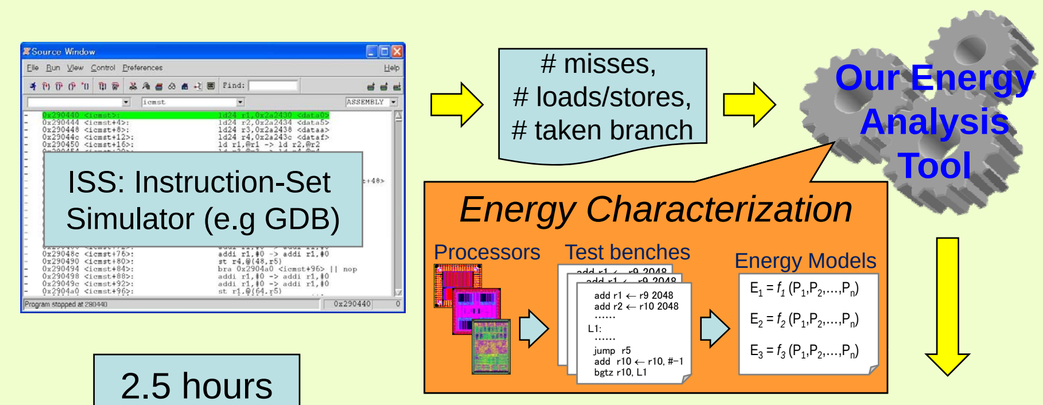


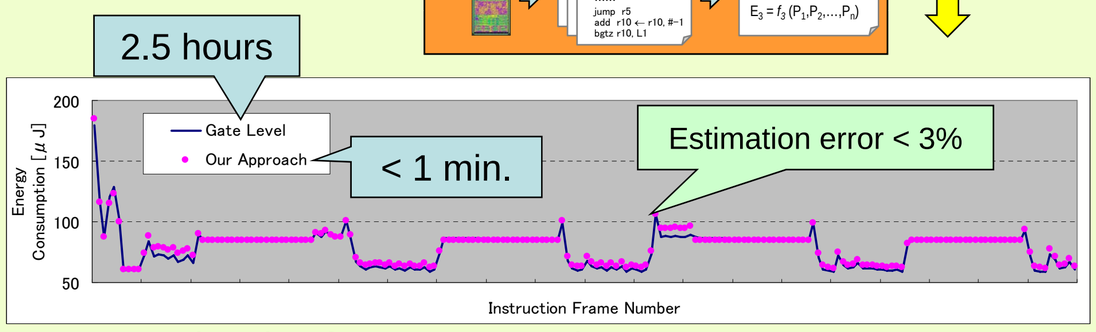
  - Nagoya Univ.
    - Hiroaki Takada (Leader)
    - Hiroyuki Tomiyama
    - 2 post-doc researchers & 3 students
  - Kyushu Univ.
    - Tohru Ishihara (Leader in Kyushu Univ.)
    - Other 2 faculty members
    - 1 post-doc researcher & 6 students
  - Toshiba Corp.
    - 6 engineers involved.

Research Topics

- **Energy Characterization/Estimation:**
  Our tool characterizes the energy consumption of processors using several parameters observed from software. Once the characterization is done, the energy of the software can be quickly estimated by using software simulators.
- **Compiler Directed Code Placement:**
  A post processor of a C compiler targeting an SH3 processor is developed. This finds the optimal locations of functions and data objects in a memory address space, which minimizes the energy consumption of the target processor.
- **Multiple-Performance Processor:**
  This processor dynamically selects a cache size and one of PE-cores which use different supply voltages from each other. This makes it possible to reduce the average power without losing the peak performance of the processor.

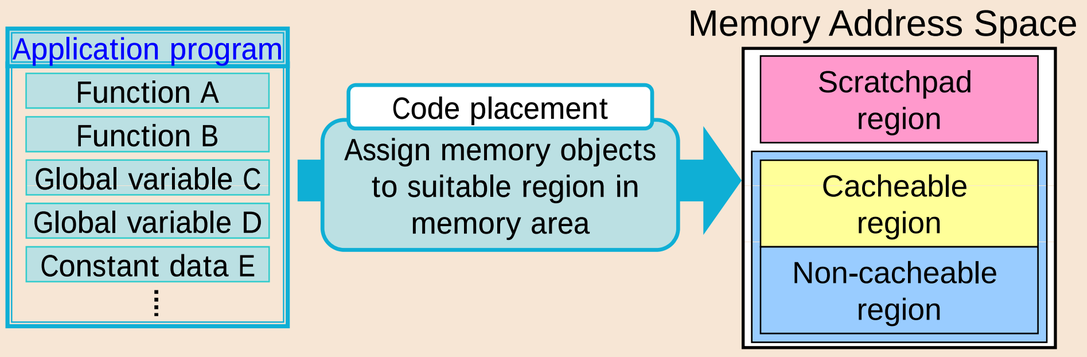
Energy Characterization Tool





Energy estimation for JPEG encoder run on a M32R-II processor

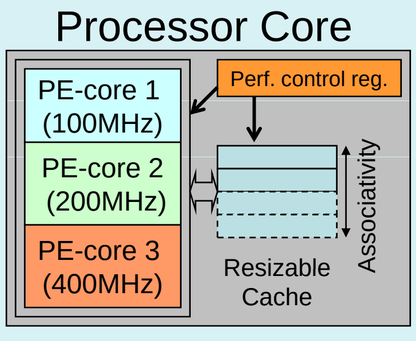
Compiler Technique; Code Placement

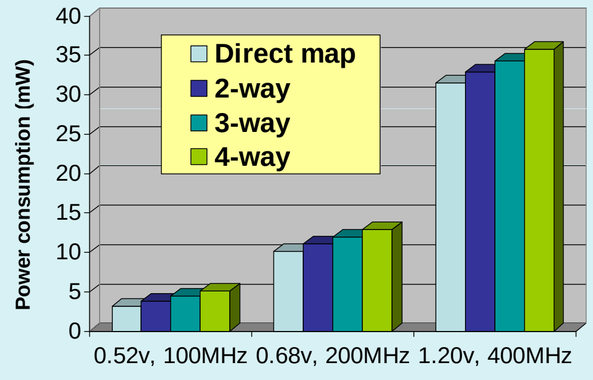


- Techniques applied simultaneously:
  1. Reduce conflict misses
  2. Use Scratch Pad Memory
  3. Bypass cache access

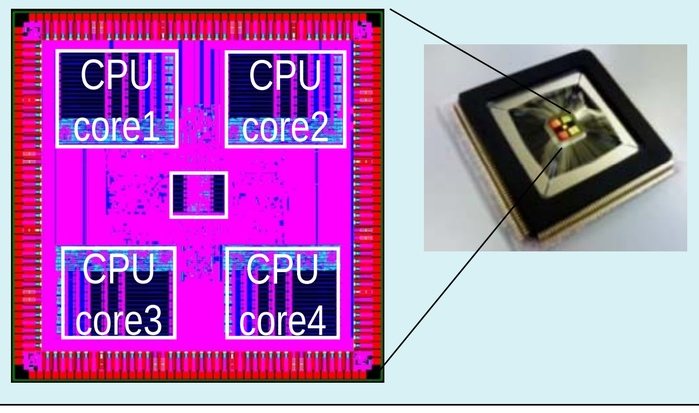
- 20% energy reduction
- No performance loss
- w/o any hardware modification

Multiple-Performance Processor





90nm Process, 5mm square



LSI IP Award